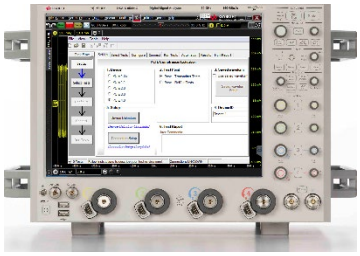
D9040PCIC PCI Express® 4.0 (Gen4) Electrical Compliance Software

for Infiniium Oscilloscope



Verify and Debug your PCI Express® Designs More Easily

Keysight Technologies, Inc. PCI Express electrical performance validation and compliance software provides you with a fast and easy way to verify and debug your PCI Express 4.0, 3.0, 2.0, and 1.1/1.0a designs for both silicon validation (as per the PCIe® BASE specification) as well as for PCI Express 3.0, 2.0, and 1.1/1.0a add-in cards and motherboard systems (as per the PCIe CEM specification). In addition, this software tool will support testing using a U.2 (SFF-8639) at speeds up to 8 GT/s.

The PCI Express electrical test software allows you to automatically execute PCI Express electrical transmitter tests, and it displays the results in a flexible report format. In addition to the measurement data, the report provides a margin analysis that shows how closely your device passed or failed each test.

The PCI Express electrical test software utilizes the prescribed test methods and algorithms as required by the PCI Express Card Electromechanical (CEM) specifications for all current PCI Express Standards through PCIe 3.0. This produces results that are not only consistent with the PCI-SIG® SigTest utility, but also provides you with a fast and easy means of executing complex two-port motherboard tests and single port add-in card test with total automation.

In addition to transmitter testing, the N5990xxA Automated Compliance and Device Characterization Test suit sets up the M8020A and M8040A jBERT for performing PCI Express receiver tests such as the CEM paragraph 2.8 and 2.10 compliance tests as well as the paragraph 2.3 and 2.4 Link Equalization Tests. Additional receiver tests include Jitter Tolerance, Sensitivity, Equalization Coefficient Matrix Scan, and Equalization Pre-Shoot De-Emphasis Scan.

The PCI Express electrical performance validation and compliance software performs a wide range of electrical tests as per the PCI Express CEM 3.0, 2.0, 1.1/1.0a electrical specifications for add-in cards and motherboard systems as documented in chapter 4 of the PCIe 3.0 base specification and chapter 4 of the PCIe 3.0 card electromechanical specification.

With the growing popularity of SSD drives, PCI Express has become the de-facto physical layer interface for solid state storage drives. One of the more common connectors used in SSDs today is the U.2 (also called the SFF-8639 connector). Using U.2 Test fixtures provided by the PCI-SIG, the Keysight PCI Express electrical test software supports the testing of U.2 based end points and root complexes at 2.5 G, 5 G, and 8 GT/s. In addition to full swing (800 mV) testing, the software also supports testing for low-power, half-swing devices (400 mV) as per the PCI Express Architecture Mobile Graphics Low-Power Addendum to the PCI Express Base Specification Revision 1.0.

KEYSIGHT

Features

The Keysight D9040PCIC PCI Express 4.0 electrical transmitter (TX) test software represents the latest PCI Express TX test tool that supports PCI Express 4.0 with speeds of up 16 GT/s. Below is a list of a few of the key features of this software package.

- PCIe 4.0 BASE TX measurements including uncorrelated TJ, DJ, and PWJ, pseudo package loss and other parameters defined in the 0.7 version of the PCI Express BASE specification.
- BASE spec TX measurements are supported at 16 GT/s, 8 GT/s, 5 GT/s, and 2.5 GT/s.
- Legacy support for PCI Express 3.x, 2.x, and 1.1 compliance tests (BASE and CEM).
- PCI 4.0 reference clock measurements as defined in v0.9 of the PCIe 4.0 BASE spec.
- Support for U.2 (SFF-8639) PCIe 3.0 CEM measurements for endpoint and root complex devices (8 GT/s, 5 GT/s, and 2.5 GT/s).
- Automated DUT control for endpoint and root complex testing using a Keysight 81150A or 81160A Pulse Function Arbitrary Noise Generator.
- New Workshop Compliance mode for rapid PCI SIG-style compliance testing including Sigtest HTIML report files.
- Support for de-embedding of test fixtures, high speeds switches and cables[1] or the embedding of channel or package model losses.
- Support for Keysight and BitifEye high speed switch networks to automate testing of multi-lane DUTs.
- Test setup wizard for ease-of-use.
- Pass/fail margin analysis.
- Two-port (explicit clock and data) supported for motherboard signal quality testing[2].
- Support for both full-swing and low-power, half-swing devices.
- Supported on Keysight UXR-Series, Z-Series, V-Series, Q-Series, X-Series, and 90000A real time oscilloscopes. Also supported for 2.5 G measurements only on the S-Series oscilloscope (See ordering information).

With the PCI Express D9040PCIC electrical test software, you can use the same oscilloscope you use for everyday debugging to perform automated testing and margin analysis based on the PCI-SIG-specified tests.

[1] Requires the purchase of the optional D9110DMBA De-Embedding or D9120ASIA Keysight InfiniiSim Advanced Waveform Transformation Toolset for Infiniium Oscilloscopes.
[2] Requires a 4 channel Oscilloscope with the required bandwidth on all 4 channels or the use of appropriate InfiniiMAX probes and SMA/3.5 mm probe head adapters.

PCI Express Compliance Testing

To pass signal quality testing at a PCI-SIG-sponsored compliance workshop, your product must successfully pass “Gold Suite” testing, based on the PCI-SIG SigTest application. The SigTest application tests your device against the minimum signal-quality performance requirements for PCIe. If you are developing receivers and transmitters for add-in boards and system motherboards, the PCI Express electrical test software helps you execute the SigTest tests and additional oscilloscope based TX tests. See the list of tests in Table 3 on page 24 (for 1.1 test coverage).

While SigTest tests provide a good overview of PCI Express electrical signal quality, it addresses only a subset of the electrical compliance measurements specified in the PCI-SIG specification. The SigTest application also provides minimal reporting capability with pass/fail indication and measurement values, and has limited debugging capabilities to decipher eye mask violations or excessive jitter.

For PCI Express 4.0 measurements, the software automatically calculates uncorrelated total jitter, uncorrelated deterministic jitter, and uncorrelated PWJ necessary for validating new PCIe 4.0 or 3.0 compliant chipsets compliant chipsets. For devices compliant with versions of PCI Express 2.0 or earlier, random jitter is also reported for completeness and a voltage margin “eye” diagram is included in the final HTML report. DJ and TJ values are specified in the PCIe 2.0 specification and are required for compliance verification compliance verification under that version of the standard.

Figure 1. PCI Express 4.0 supports data rates up to 16 GT/s as shown above (P4 preset)

Benefits

PCI Express electrical test software benefits

The PCI Express electrical test software saves you time by setting the stage for automatic execution of PCI Express electrical tests. Part of the difficulty of performing electrical tests for PCI Express is hooking up the oscilloscope, loading the proper setup files, and then analyzing the measured results by comparing them to limits published in the specification. The PCI Express electrical test software does much of this work for you. In addition, if you discover a problem with your device, robust debug tools are available to aid in root-cause analysis. Tools are provided by the Keysight E2688A high-speed serial data analysis software, which you must install on your oscilloscope to use the PCI Express electrical test software.

The software also now has an integrated interface for controlling the InfiniiSim Waveform Transformation Toolset for de-embedding of test fixtures. Introduced with PCIe 2.0 and also required under the PCIe 3.0 and 4.0 standards, de-embedding of test fixtures utilizes S-parameters as input to create a de-embed model that helps to restore high frequency signal content that is often lost or significantly attenuated by test fixtures and cables.

This can help to recover significant jitter margin normally lost to fixtures used in a test setup. The InfiniiSim Waveform Transformation Toolset can also be used to embed package model losses, channel losses, or a combination of both package and channel losses together. This can be useful for determining end of channel characteristics of your PCIe signal.

The PCI Express electrical test software offers many more electrical tests than the SigTest application. PCI Express electrical test software automatically configures the oscilloscope for each test, and it provides an informative results report that includes margin analysis indicating how close your product is to passing or failing a particular test assertion. Table 1 shows a side-by-side comparison of the capabilities of the SigTest application and the Keysight PCI Express electrical test software. A list of the measurements made by the PCI Express electrical test software can be found in Table 3, (Table 3 contains comparison of SigTest vs. Keysight).

Capabilities	Keysight PCI Express software	PCI-SIG SigTest
Support for PCIe 4.0	BASE Spec	BASE Spec
Integrated de-embedding support or the embedding of channel or package loss	Yes (InfiniiSim waveform transformation toolset required)	Varies with version level of PCIe std.
Number of measurement assertions	Up to 47	4
Support for PCIe CEM 1.0a, 1.1, 2.0, 3.0 Support for U.2 2.5G, 5G, and 8G	Yes	Yes
Reference clock tests	12 (1.1, 2.0, 3.0) 13 (4.0)	0[3]
Automated oscilloscope setup for each measurement	Yes, guided	No, single setup
Measurement results	Pass/fail with margin analysis	Pass/fail with measured value
CEM based measurement methodology	Yes	Yes
Clock recovery method	PCI-SIG SigTest or 1st/2nd order PLL	PCI-SIG SigTest
Brick wall filter (2.0 testing)	Yes	Yes
Custom HTML report generation	Yes	No
Support for low power device	Yes	No
Selectable number of tests performed	Yes	No
Multi-trial run support	Yes	No
Debug mode for “what if” analysis	Yes	No
Compliance test boards supported	CBB1-4 CLB1-4, U.2 CBB	CBB1-4 CLB1-4, U.2 CLB

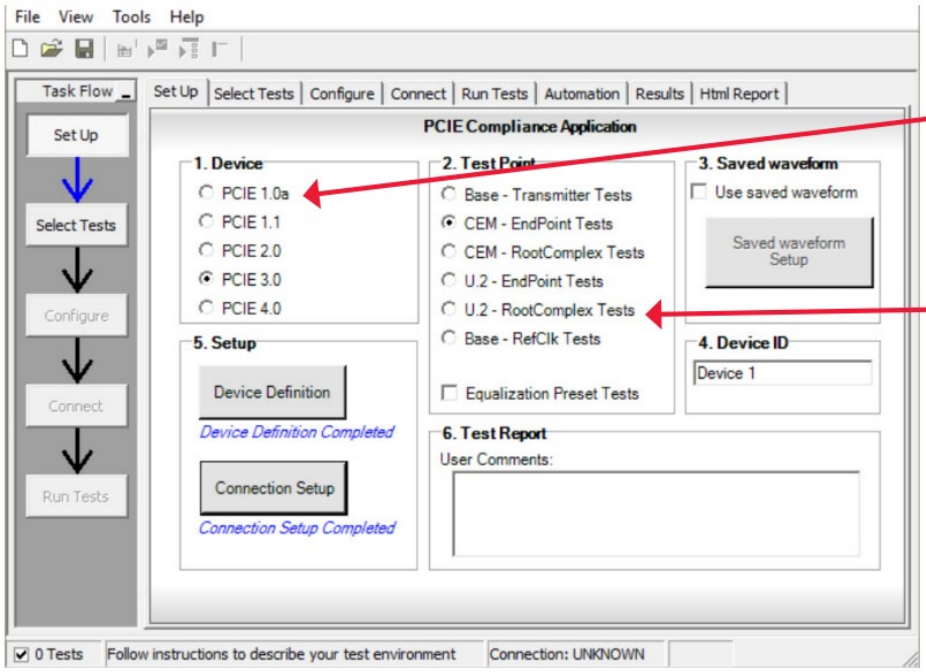
Table 1. Comparison of capabilities of the Keysight PCI Express electrical test software and the PCI-SIG SigTest application.

[3] PCI-Sig offers a separate utility (Clock Jitter) for analyzing reference clock phase jitter.

Easy Test Definition

The PCI Express electrical test software extends the ease-of-use advantages of Keysight's Infiniium oscilloscopes to testing PCI Express designs. The Keysight automated test engine walks you quickly through the steps required to define the tests, set up the tests, perform the tests, and view the test results. You can select a category of tests all at once, or specify individual tests. You can save tests and configurations as project files and recall them later for quick testing and review of previous test results. Straightforward menus let you perform tests with a minimum of mouse clicks.

The software allows you to easily specify the test standard you want to use to test the compliance of your device. This makes test setup easy as only the appropriate tests for the test point you pick are shown on later test selection pages.



Pick the standard you want to test against

Choose the test point or specific signal you want to test

Figure 2a. The software allows you to easily specify the test standard you want to use to test the compliance of your device. This makes test setup easy as only the appropriate tests for the test point you pick are shown on later test selection pages.

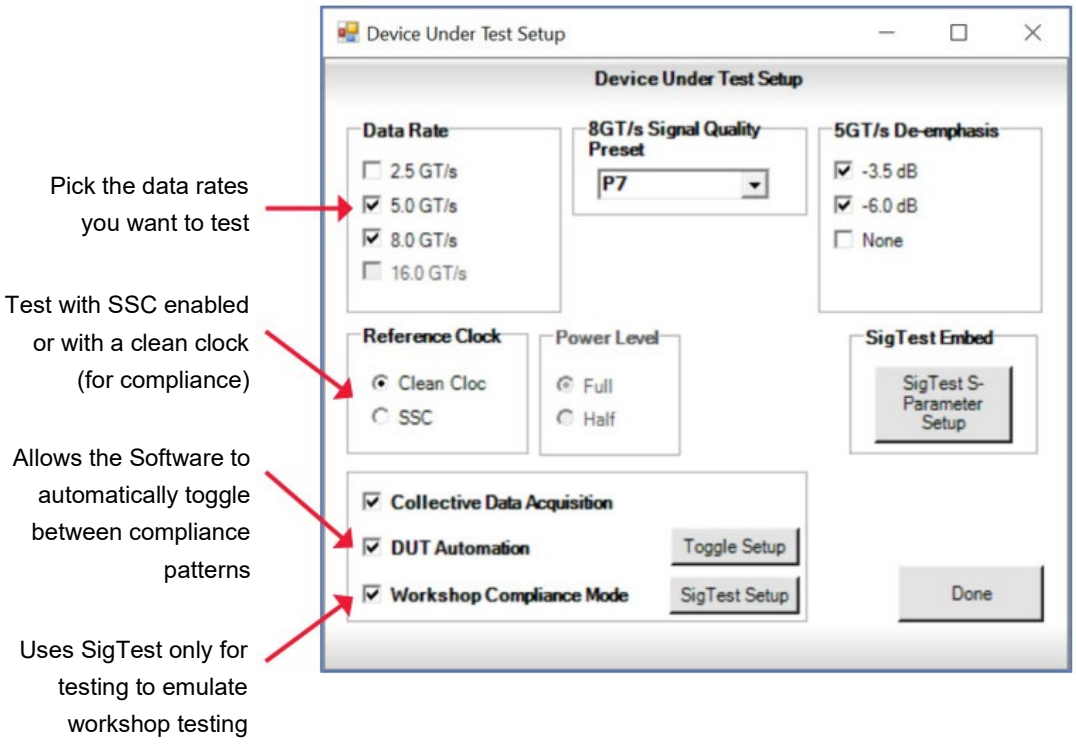


Figure 2b. The Device Definition dialog allows the selection of the data rates to be tested, testing with SSC enabled or a clean clock, Automatic toggling of compliance patterns, testing with SigTest, and more

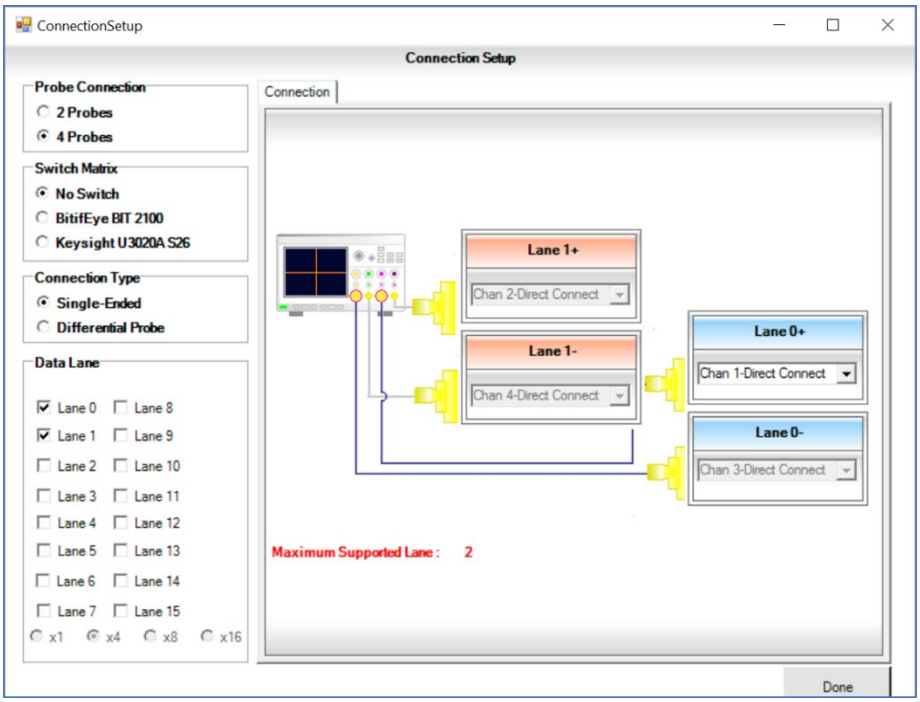


Figure 2c. The Connection Setup dialog allows the user to setup multiple lane testing. One or two lanes can be tested with the scope alone but all the lanes will be documented. This testing can be automated with the use of switches available from Keysight or BitifEye

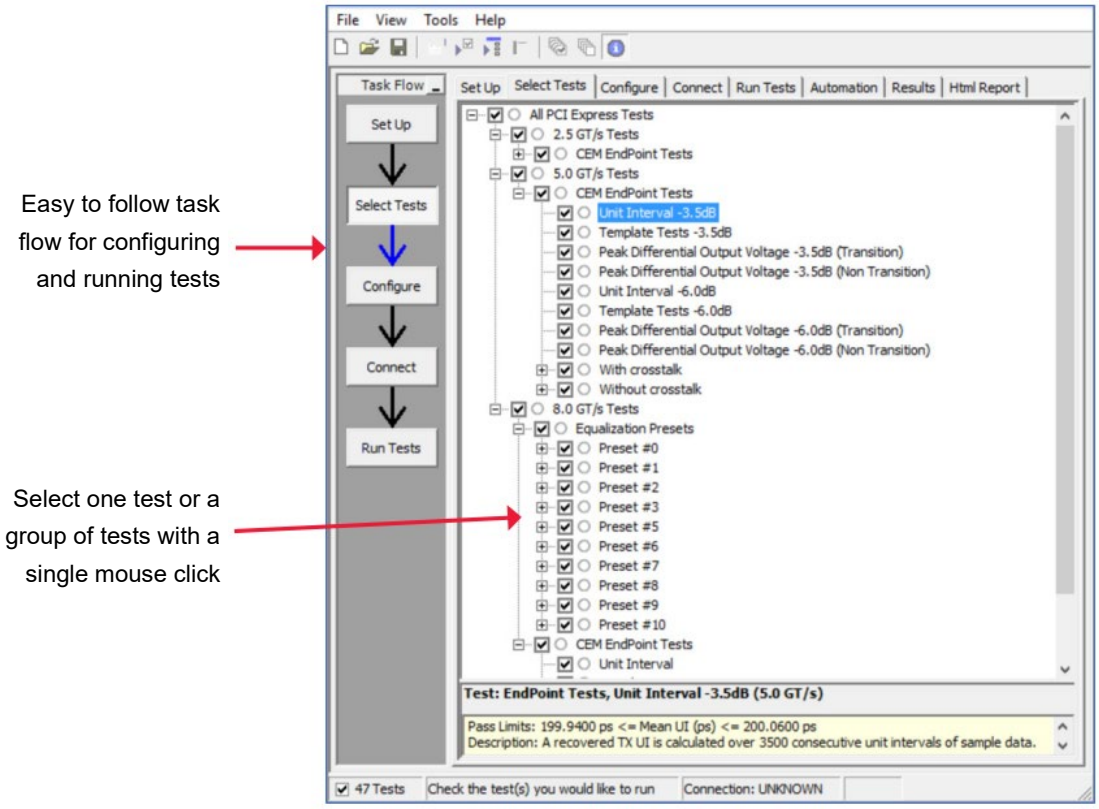


Figure 3. The Keysight automated test engine guides you quickly through selecting tests, configuring tests, setting up the connection, running the tests, and viewing the results. Individual tests or groups of tests are easily selected with a mouse click

PCI Express 4.0

The D9040PCIC compliance application includes support for testing PCI Express 4.0 integrated circuits. The tests supported are shown below in Figure 4. This specification elevates the data rate for PCIe 4.0 devices to 16 GT/s. This results in a maximum throughput of approximately 15.8 Gb/s per lane (taking into account encoding overhead). PCIe 4.0 shares many elements in common with PCIe 3.0 including 128/130 bit encoding. Nevertheless, at 16 GT/s, the signal is significantly attenuated by a typical FR4 channel which increases the importance of ensuring your design has the best signal integrity possible. With Keysight oscilloscopes, you are ensured of using instruments with the lowest noise floor in the industry which helps to ensure you will perform your compliance tests with the greatest margin possible.

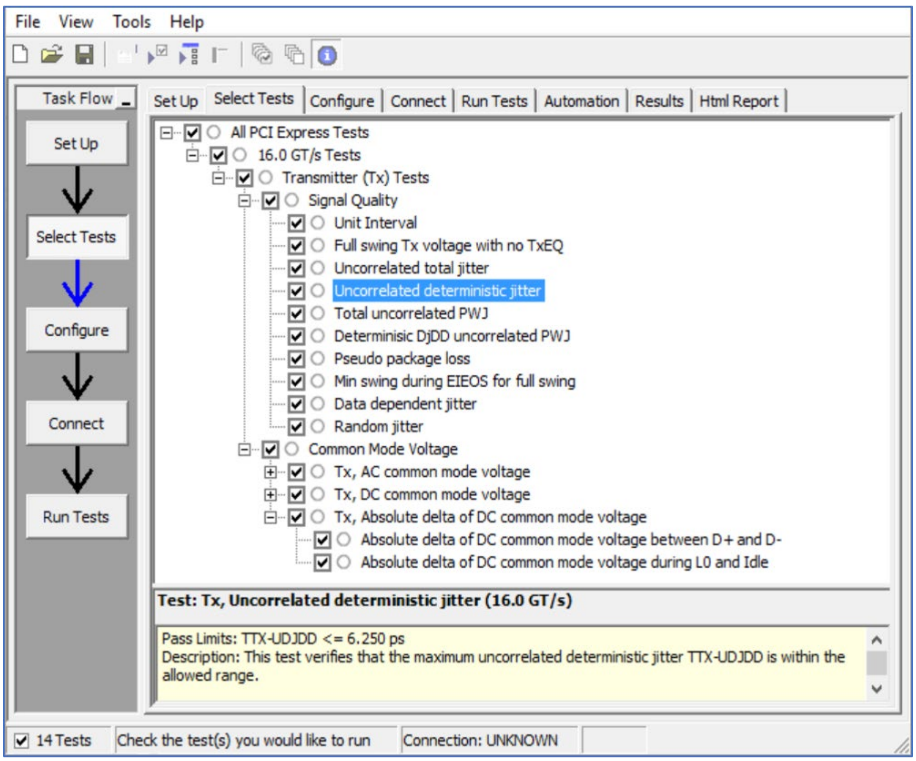


Figure 4. PCI Express 4.0 BASE Specification transmitter tests

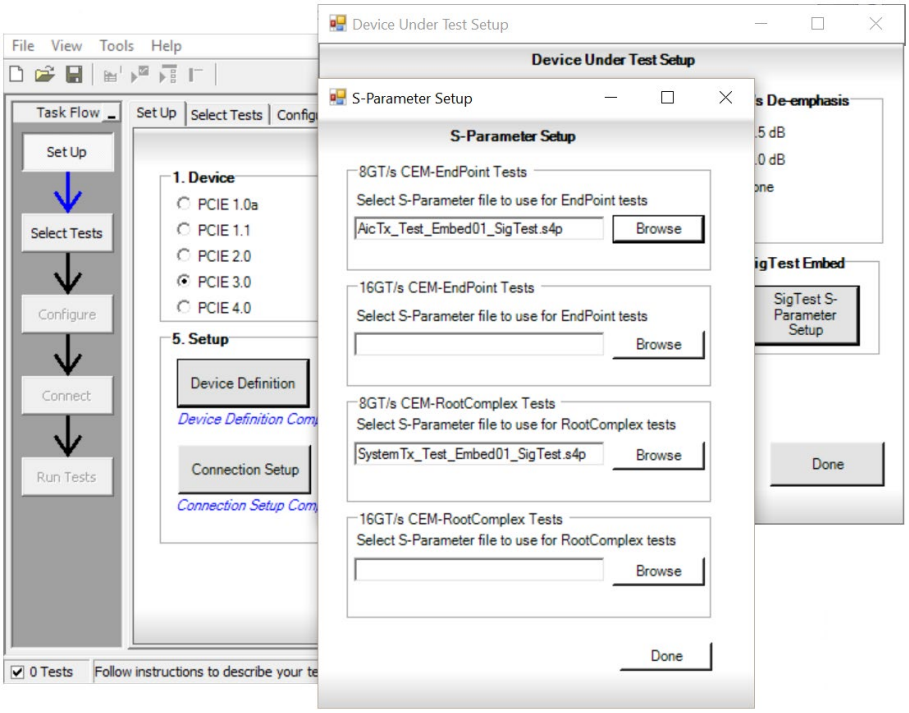


Figure 5. The D9040PCIC provides the option to use a user provided S-Parameter file S-Parameter file for 8 GT/s CEM testing

PCI Express U.2

The D9040PCIC compliance application includes support for testing PCI Express U.2 Devices and Hosts using the PCI-SIG U.2 CBB and CLB shown in Figure 6. This includes the same Gen3 2.5, 5.0, and 8.0 Gbps tests as with CEM Add-in cards and Systems. Your device will be tested to the parameters specified for U.2 devices. And with Keysight oscilloscopes, you benefit from using instruments with the lowest noise floor in the industry which helps to ensure you will perform your compliance tests with the greatest margin possible.

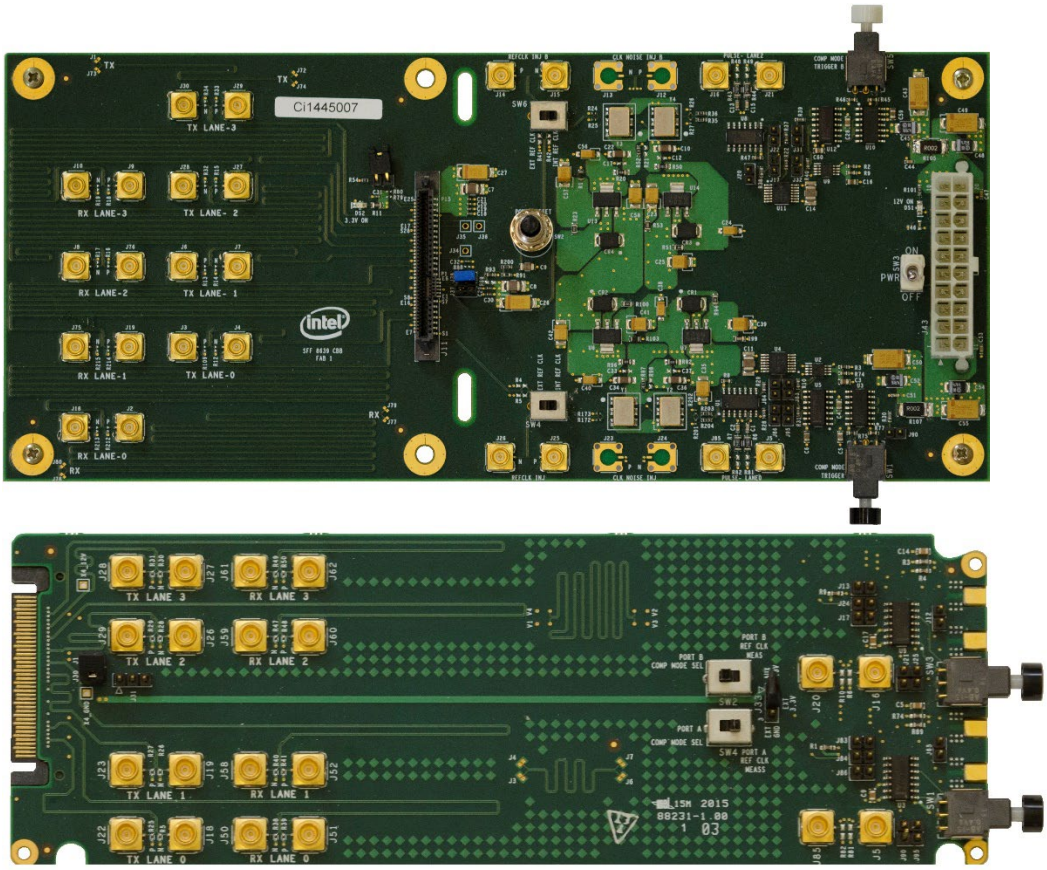
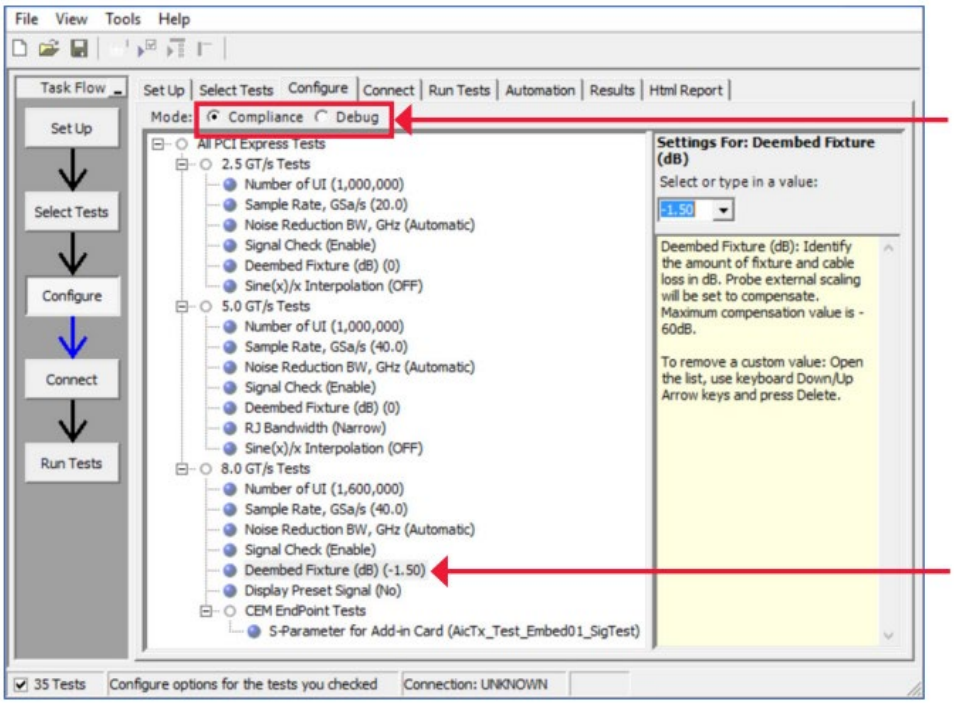


Figure 6. PCI-SIG U.2 CBB and U.2 CLB

Configurability and Guided Connections

The PCI Express electrical test software provides flexibility in your test setup. It guides you to make connection changes with hookup diagrams when the tests you select require it. All PCI Express electrical compliance tests you perform are based on the official PCI-SIG approved set of test fixtures. The compliance fixtures include the Compliance Base Board (CBB3) for add-in card testing, and the Compliance Load Board (CLB3) for motherboard or system testing. Connection to the compliance test fixtures is selectable between SMA/SMP cables or Keysight InfiniiMax active differential probes.



Run tests in Compliance or Debug mode. Debug mode allows more configuration options when investigating a test failure

Configure allows the setting of test options like De-embedding test fixtures

Figure 7. In the Configure tab you can set parameters like number of UI, noise reduction, signal check, etc.

If more than one test setup connection is required, you will be notified here

You are prompted to make the appropriate connections for the set of tests

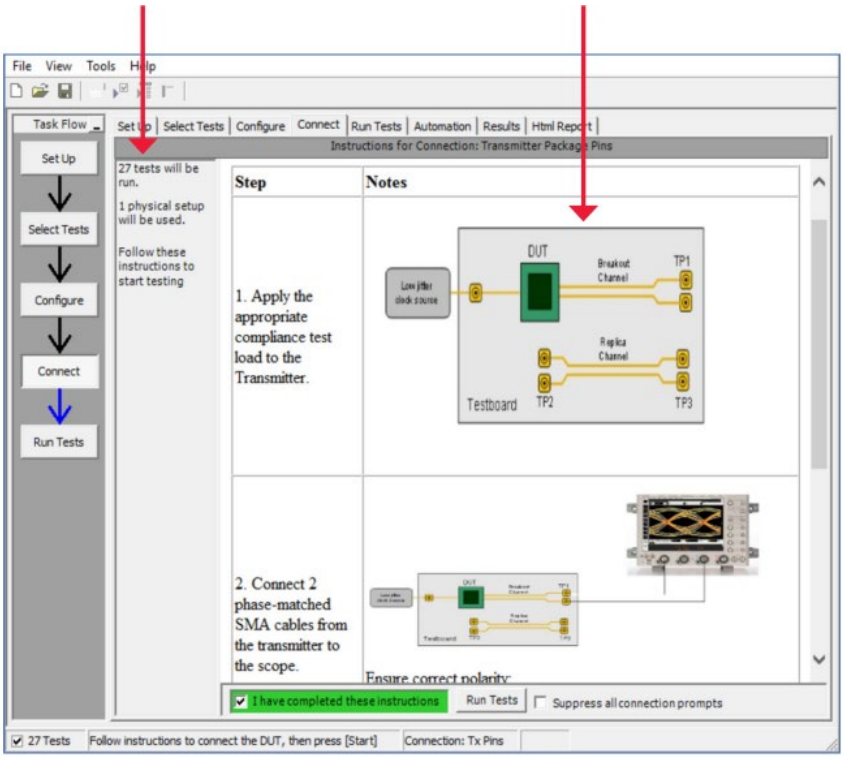
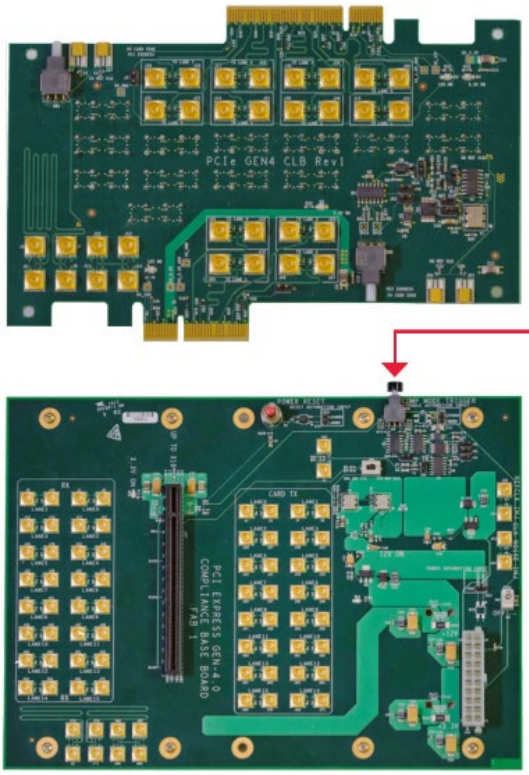


Figure 8. When you make multiple tests where the connections must be changed, you are prompted with connection diagrams and/or photographs

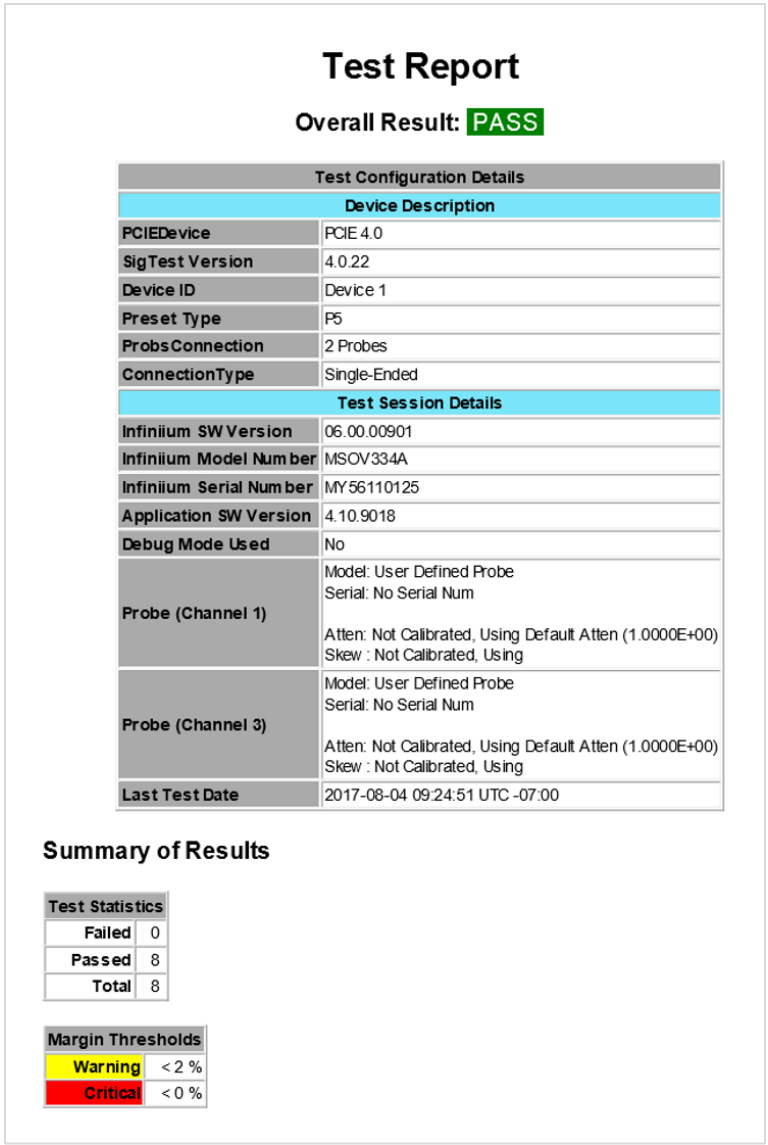


Toggle circuit to switch between 2.5, 5, 8, and 16 Gb/s. This Toggle can be automated as well.

Figure 9. Shown here are the proposed PCI-SIG Compliance Base Board the PCI-SIG Compliance Base Board (CBB4) for Gen4 add-in card testing, and the Compliance Load Board (CLB4) for Gen4 motherboard or host system testing

Reports with Margin Analysis

In addition to providing you with measurement results, the PCI Express electrical test software provides a report format that shows you not only where your product passes or fails, but also reports how close you are to the limits specified for a particular test assertion. You can select the margin test report parameter, which means you can specify the level at which warnings are issued to alert you to electrical tests where your product is operating close to the official test limits defined by the particular version of the PCI Express specification you are testing.



Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
PCIEDevice	PCIE 4.0
SigTest Version	4.0.22
Device ID	Device 1
Preset Type	P5
ProbsConnection	2 Probes
ConnectionType	Single-Ended
Test Session Details	
Infiniium SW Version	06.00.00901
Infiniium Model Number	MSOV334A
Infiniium Serial Number	MY56110125
Application SW Version	4.10.9018
Debug Mode Used	No
Probe (Channel 1)	Model: User Defined Probe Serial: No Serial Num Atten: Not Calibrated, Using Default Atten (1.0000E+00) Skew : Not Calibrated, Using
Probe (Channel 3)	Model: User Defined Probe Serial: No Serial Num Atten: Not Calibrated, Using Default Atten (1.0000E+00) Skew : Not Calibrated, Using
Last Test Date	2017-08-04 09:24:51 UTC -07:00

Summary of Results

Test Statistics	
Failed	0
Passed	8
Total	8

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Figure 10. The PCI Express electrical test software results report documents your test, indicates the pass/fail status, the test specification range, the measured values, and shows how much margin you have

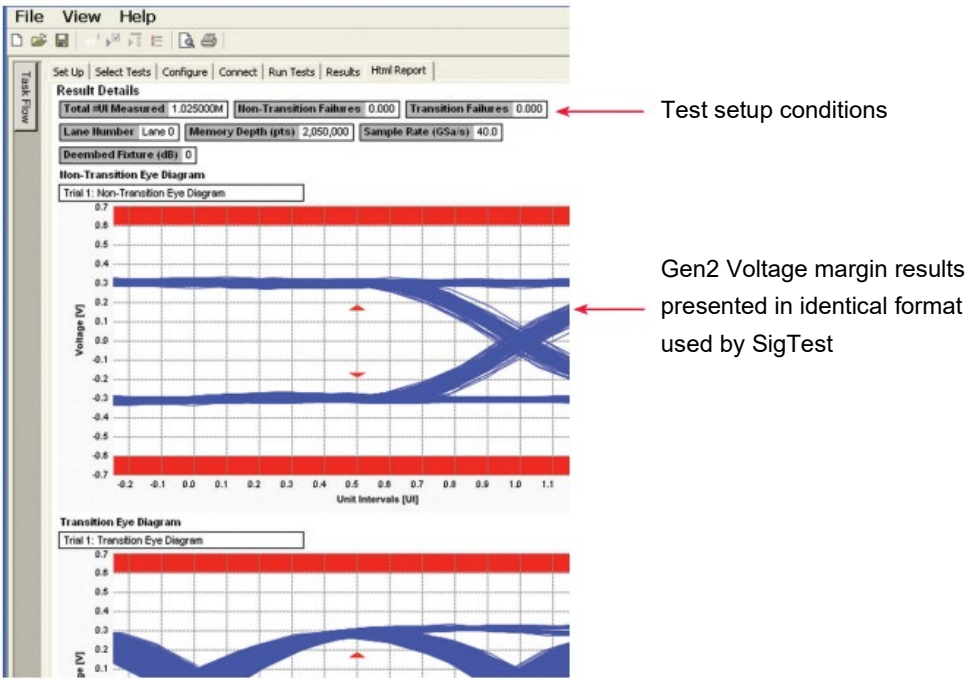


Figure 11. The HTML report provides additional details including test setup conditions, graphical results, and test limits (where appropriate)

Summary of Results

Test Statistics	
Failed	0
Passed	8
Total	8

Margin Thresholds	
Warning	<2 %
Critical	<0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	Tx, Unit Interval (16.0 GT/s)	62.5044 ps	38.3 %	62.4812 ps <= VALUE <= 62.5188 ps
✓	0	1	Tx, Uncorrelated total jitter (16.0 GT/s)	8.063 ps	35.5 %	VALUE <= TTX_UTJ_Limits
✓	0	1	Tx, Uncorrelated deterministic jitter (16.0 GT/s)	290 fs	95.4 %	VALUE <= 6.250 ps
✓	0	1	Tx, Total uncorrelated PWJ (16.0 GT/s)	10.442 ps	16.5 %	VALUE <= 12.500 ps
✓	0	1	Tx, Deterministic DJDD uncorrelated PWJ (16.0 GT/s)	840 fs	83.2 %	VALUE <= 5.000 ps
✓	0	1	Tx, Pseudo package loss (16.0 GT/s)	-7.889 dB	363.0 %	VALUE <= 3.000 dB
		1	Tx, Data dependent jitter (16.0 GT/s)	15.427 ps		Information Only
		1	Tx, Random jitter (16.0 GT/s)	7.778 ps		Information Only

Figure 12. How close you are to passing or failing a test is indicated as a % in the margin field. A result highlighted in yellow or red indicates that the margin threshold level for a warning or failure was detected

Extensibility

You may add additional custom tests or steps to your application using the User Defined Application (UDA) development tool (http://www.keysight.com/find/uda). Use UDA to develop functional “Add-Ins” that you can plug into your application.

Add-ins may be designed as:

- Complete custom tests (with configuration variables and connection prompts)
- Any custom steps such as pre or post processing scripts, external instrument control and your own device control

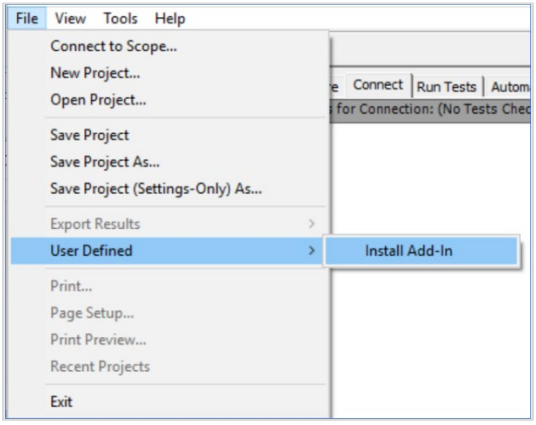


Figure 13. Importing a UDA Add-In into your test application

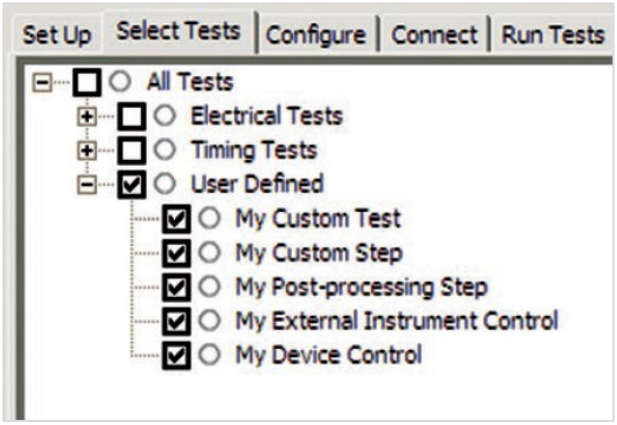


Figure 14. UDA Add-In tests and utilities in your test application

Automation

You can completely automate execution of your application's tests and Add-Ins from a separate PC using the Remote Programming Interface feature. You can create and execute automation scripts right inside the application using a convenient built-in client.

The commands required for each task may be created using a command wizard or from "remote hints" accessible throughout the user interface.

Using automation, you can accelerate complex testing scenarios and even automate manual tasks such as:

- Opening projects, executing tests and saving results
- Executing tests repeatedly while changing configurations
- Sending commands to external instruments
- Executing tests out of ord

Combine the power of built-in automation and extensibility to transform your application into a complete test suite executive:

- Interact with your device controller to place it into desired states or test modes before test execution.
- Configure additional instruments used in your test suite such as a pattern generator and probe switch matrix.
- Export data generated by your tests and post-process it using your favorite environment, such as MATLAB, Python, LabVIEW, C, C++, Visual Basic etc.
- Sequence or repeat the tests and "Add-In" custom steps execution in any order for complete test coverage of the test plan.

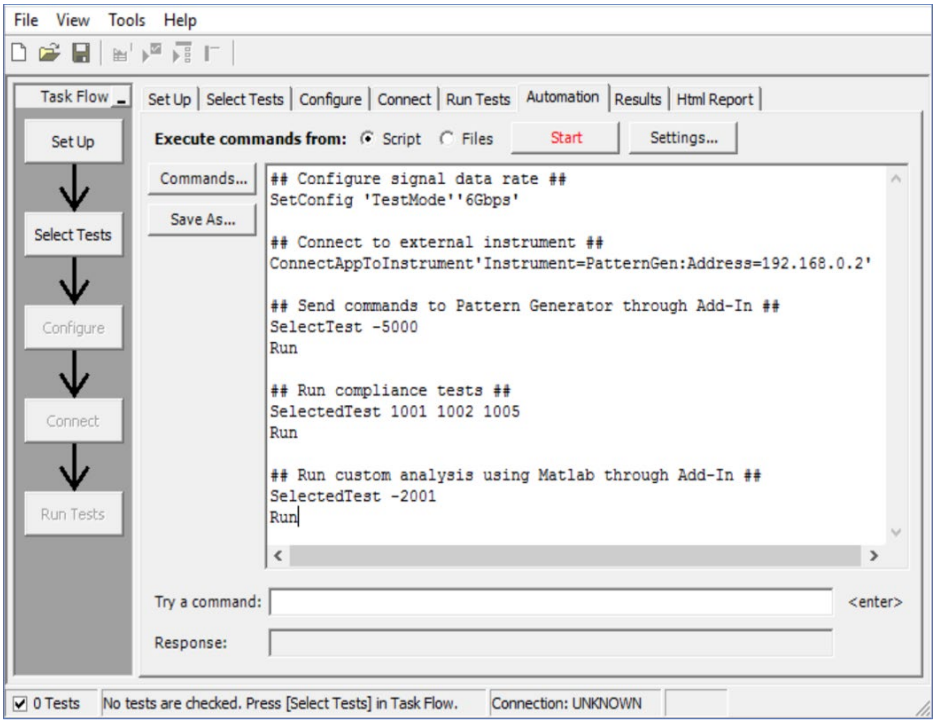


Figure 15. Remote Programming script in the Automation tab

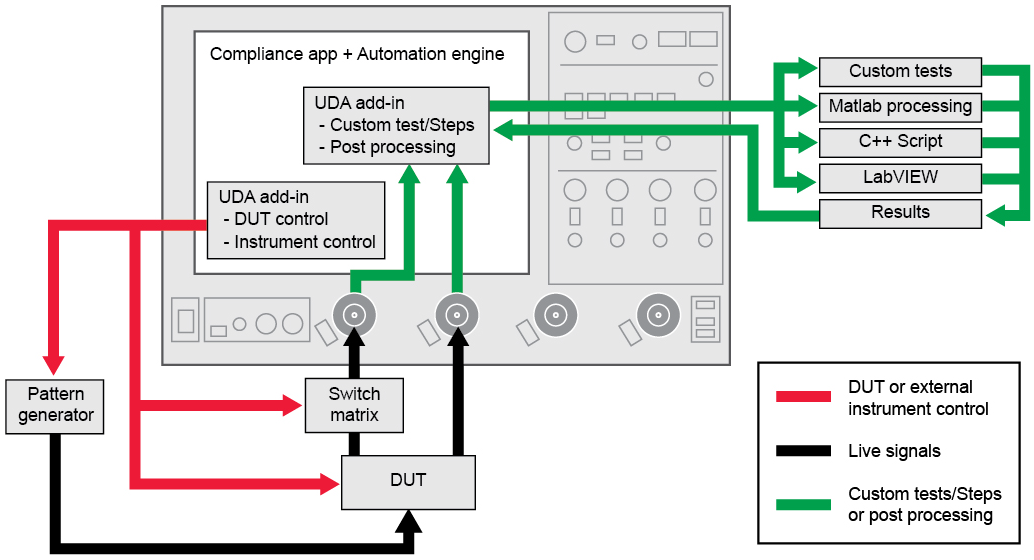


Figure 16. Combine the power of built-in automation and extensibility to transform your application into a complete test suite executive

Switch Matrix

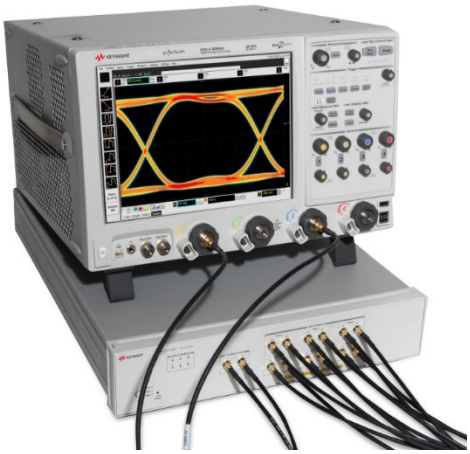


Figure 17. Automated testing for multi-lane digital bus interface through switching solution

The Keysight D9040PCIC PCI Express Compliance application, used together with switch matrix hardware, enables fully automatic testing for a multi-lane implementation of the PCIe bus. The benefits of this automated switching solution include:

- Eliminate reconnections, which saves time and reduces errors through automating test setup for each lane of a multi-lane bus.
- Maintain accuracy with the use of unique D9110DMBA De-embedding and InfiniiSim software to compensate for switch path losses and skew.
- Customize testing by using remote programming interface and the user-defined application tool for device control, instrument control and test customization.

For information of the switching solution and configuration, visit http://keysight.com/find/switching and Keysight U3020AS26 Switching Test Set product page.

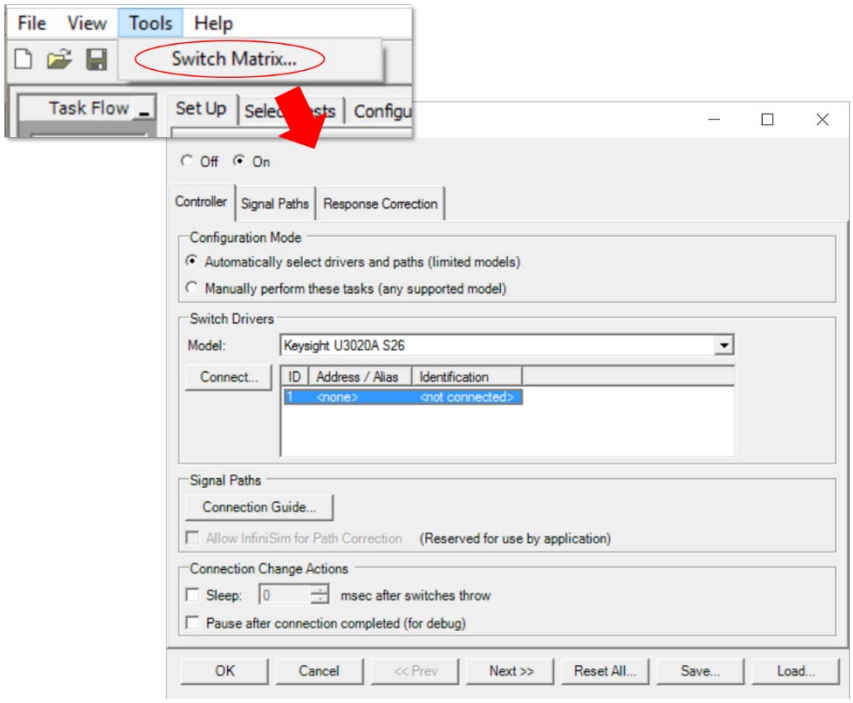


Figure 18. Switch matrix software feature enabled in the compliance application

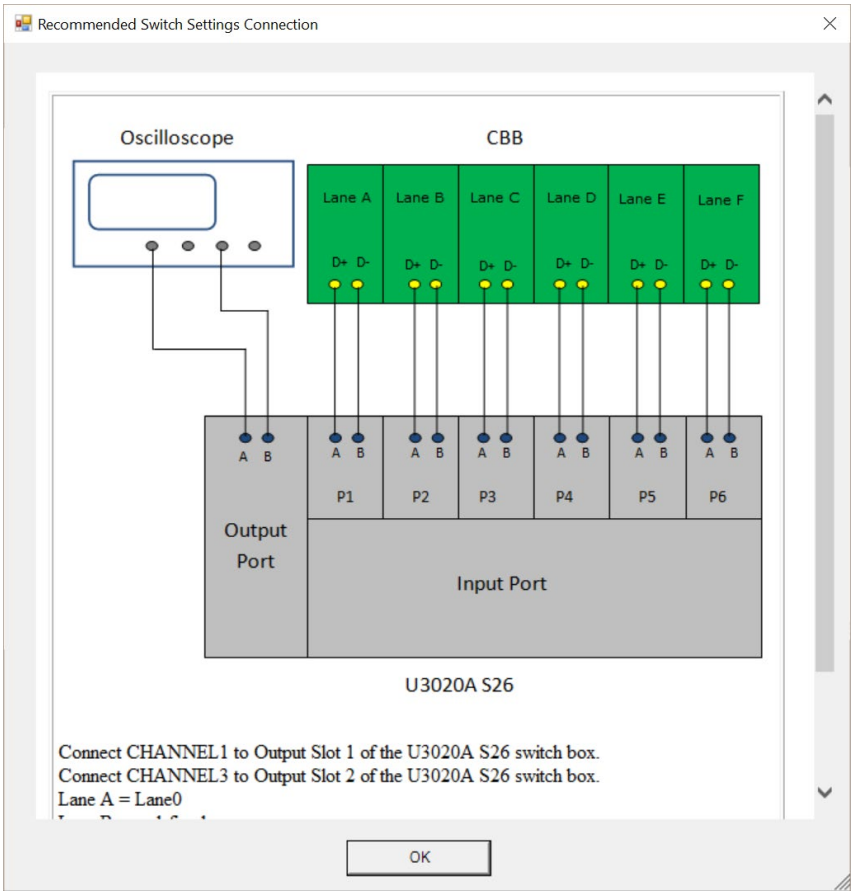


Figure 18a. A connection diagram is provided to help setup the switch

Reference Clock Measurements

The PCI Express 1.0a specification failed to specify the TX PLL loop bandwidth of the reference clock receiver or phase jitter of the reference clock itself. This is important because jitter that lies within the loop bandwidth the receiver PLL for the reference clock will transfer onto the high speed data lines. This hole in the PCI Express specification was corrected in the 1.1 version of the PCIe specification.

The D9040PCIC includes powerful reference clock evaluation tools including phase jitter. The PCIe 1.1 specification calls for a very specific phase jitter filter that focuses the measurement on the jitter that lies between 1.5 and 22 MHz. The filter also amplifies the jitter 3 dB (peaking) within this region. The Keysight D9040PCIC includes proprietary filtering software the that exactly implements the significantly expanded phase jitter filters specified in the PCI Express 4.0 Specification. The D9040PCIC also includes reference clock tests based on the PCIe 2.0 and 3.0 specification.

Utilizing Keysight's InfiniiMax 1169A or InfiniiMax III/III+ N2802A high performance differential probes, or direct cabled connections, you can measure your reference clock using the test fixture, compliance load, and probing requirements specified in the PCI Express 4.0 BASE specification.

- Reference clock tests
- Phase jitter
- Rising edge rate
- Falling edge rate
- Differential input high voltage
- Differential input low voltage
- Average clock period
- Duty cycle

Reference clock test connection using PCI Express 4.0 Test setup, load, and probe requirements.

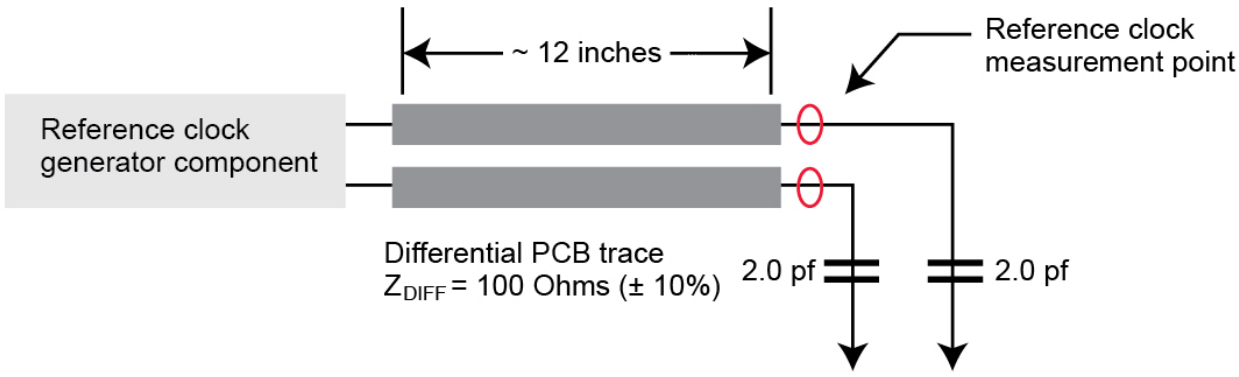


Figure 19. This figure shows the reference clock compliance channel, compliance load, and probing requirement for all PCIe 4.0 reference clock tests. Note that these tests are intended to be used to validate your PCIe reference clock at the component level

Powerful Debugging Aids

If your device fails a test, you need to determine how it failed. To use the PCI Express electrical test software, you must install Keysight's high-speed serial data analysis software, which provides you with several powerful debugging tools. Clock recovery allows you to produce an eyediagram of your data. And mask creation and testing is provided as well.

Installing the optional D9010PCIP Protocol decode tool provides 8b/10b or 128b/130b decoding that allows you to identify data-dependent errors that result in eye mask violations caused by inter-symbol interference (ISI). You can perform 8b/10b decoding to capture and display serial data synchronized with the analog view of a serial data stream (For PCIe 1.x and 2.x). The D9010PCIP Protocol Decode Tool also supports the decoding of 8G and 16G PCIe data under the PCIe 4.0 and PCIe 3.0 standard.

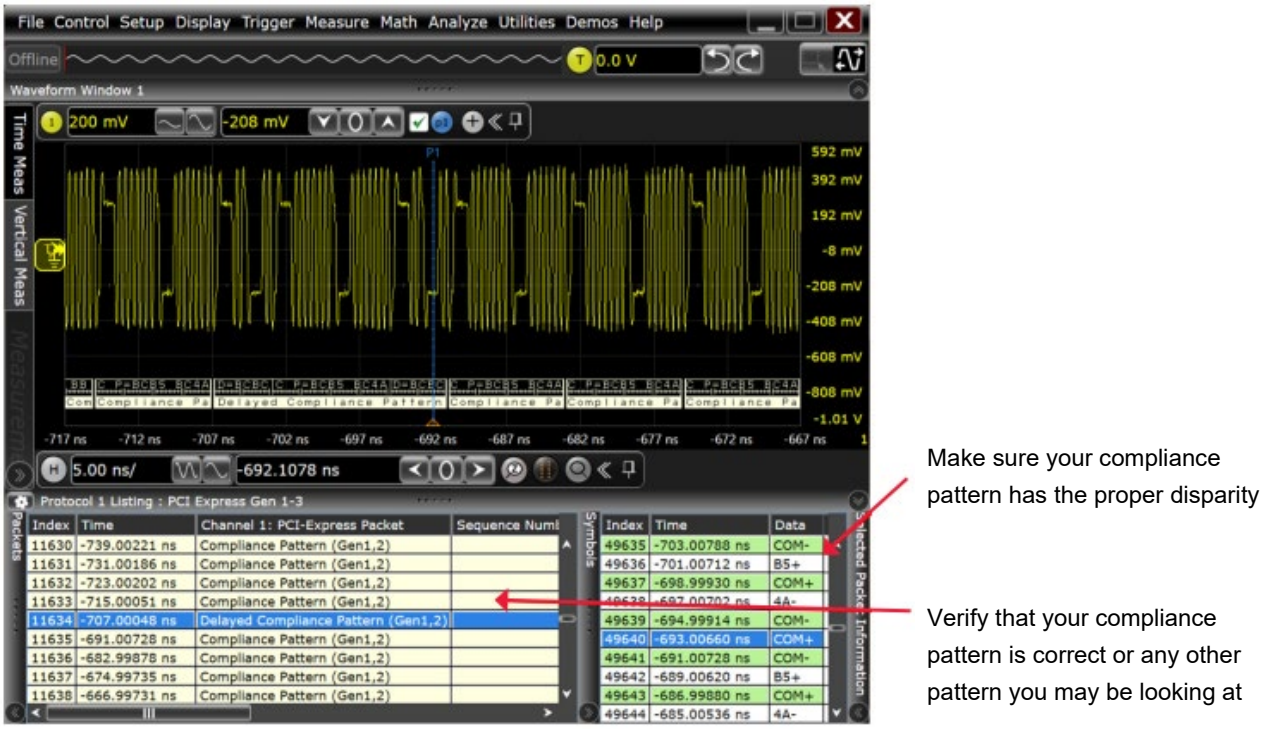


Figure 20. The N5463A provides 8b/10b and 128b/130b decode below

Using the Serial Data Analysis tool you can test for illegal characters in your compliance pattern. You can also use the mask test feature to identify the specific digital patterns that caused a specific failure in the eye diagram when testing under the 1.1 specification (using a first order PLL).

For 2.0 testing you can use a first or second order PLL for clock recovery and apply a TIE brick wall filter to achieve a proper clock filtering. For PCIe 3.0, you can use a standard 1st order PLL for clock recovery. If you are testing with SSC enabled, you will need to use a 2nd order PLL for clock recovery or use an explicit clock reference.

Figure 21. The Serial Data Analysis and optional D9120ASIA Equalization applications allow for the equalization of impaired 8 and 16 Gb/s signals so a clock can be recovered and mask testing can be performed on your waveforms

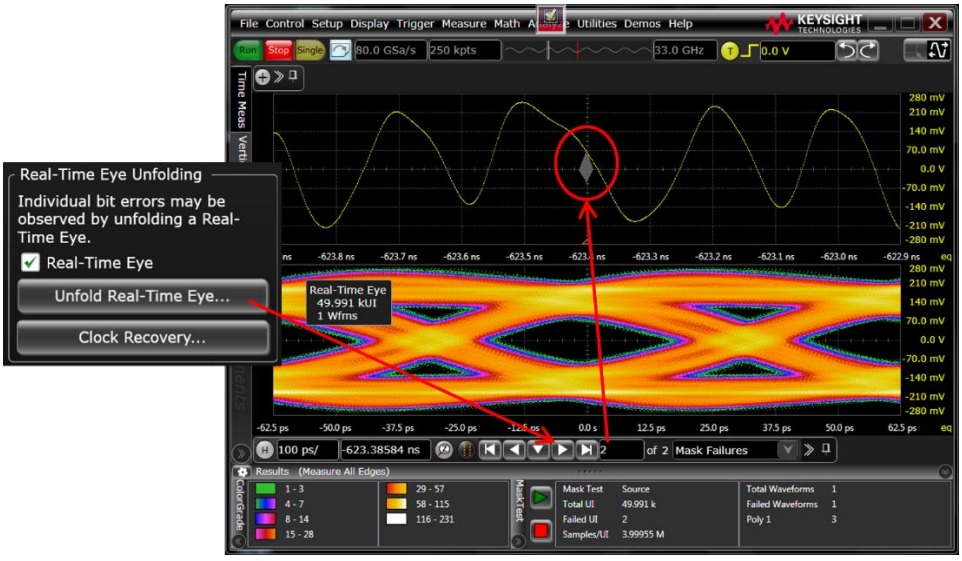


Figure 22. Once the mask test is complete the Serial Data Analysis application allows you to show the specific signal within the waveform that caused failures

Measurement Requirement

The PCI Express electrical performance validation and compliance software require one of the PCISIG approved compliance test fixtures (CBB or CLB) and at least two SMA/3.5 mm cables in order to run tests. Alternatively you can also InfiniiMax or InfiniiMax III/III+ differential probes, SMA/3.5 mm differential probe heads having the bandwidth appropriate to the maximum PCIe data rate you plan to measure. The D9040PCIC also requires the D9110DMBA (or D9120ASIA) to de-embed test traces or to embed trace and package model losses for PCIe 4.0 measurements. Some measurements cannot be made with the PCISIG compliance tet fixtures and may require you to build or acquire a custom test board, assembly or other test fixture.

To purchase the PCI Express compliance test fixtures, consult the PCI-SIG Web site and select the PCI-SIG specification order form link at: www.pcisig.com/specifications/ordering_information

Compliance test fixture	Description
CBB	PCI Express Compliance Base Board for testing PCI Express add-in cards
CLB	PCI Express Compliance Load Board for testing PCI Express platforms
CBB2	Gen2 PCI Express Compliance Base Board for testing PCI Express add-in cards
CLB2	Gen2 PCI Express Compliance Load Board for testing PCI Express platforms
CBB3	Gen3 PCI Express Compliance Base Board for testing PCI Express add-in cards
CLB3	Gen3 PCI Express Compliance Load Board for testing PCI Express platforms
CBB4	Gen4 PCI Express Compliance base board for testing PCI Express CEM based, add-in cards
CLB4	Gen4 PCI Express Compliance Load board for testing PCI Express CEM based platforms
U-2 Pair	U.2 (SFF-8639) Pair: Compliance Base Board and Compliance Load Board

Bandwidth requirements for PCI Express 4.0, 3.0, 2.0, and 1.1

PCI Express operates at 2.5 GT/s, 5 GT/s, 8 GT/s and 16 GT/s. The two tables below provide guidelines on the minimum bandwidth and sample rate recommended for PCI Express Transmitter measurements. In addition to transmitter measurements, phase jitter measurements of the PCIe 100 MHz reference clock also call for a minimum sample rate used to measure the clock as is also shown below. Use this information to help you select the proper oscilloscope for your specific requirements. Also remember that receiver testing requires adequate bandwidth to ensure the most accurate calibration of your bit error ratio tester (BERT). Automated receiver calibration using the N5990xxA Automated Compliance and Device Characterization tool and the Keysight M8020A or M8040A J-BERT high performance BERT includes integration and control of Keysight high performance oscilloscopes for fast BERT calibration for receiver stressed jitter and stressed voltage testing.

PCI Express bandwidth requirements by data rate for transmitter measurements and RX calibration (PCIe 3.0 and 4.0)

Data rate	Bandwidth required	Minimum sample rate
2.5 GT/s	6 GHz	20 GSa/s
5 GT/s	12 GHz	40 GS/s
8 GT/s	12 GHz	40 GS/s
16 GT/s	25 GHz	80 GSa/s

PCI Express sample rate requirements for reference clock measurements

PCIe standard	Minimum sample rate
1.1	20 GSa/s
2.x	20 GSa/s
3.x	20 GSa/s
4.0	20 GSa/s

Recommended Test Accessories

To complete your test setup, Keysight provides a wide range of cables, adapters, terminations, etc.

Note: While the PCI-SIG does supply Gen2, Gen3, and Gen4 test fixtures for motherboard and add-in card testing, you will need to obtain SMP cables, adapters and terminators from a vendor of your choice as the SIG does not supply them.

Model number	Description
Add-in card testing	
PCI-SIG Compliance Base Board (order from www.pcisig.com/specifications/ordering_information)	
ST1847 (www.fairviewmicrowave.com) or equivalent	SMP 50 Ω terminators, one pair for all CBB lanes not probed
N2823A	Phased-matched cable pair, 2.92 mm, 1 m length, 35 GHz
80350960 (Huber+Suhner)	Two SMA-SMP minibend cables
	One PC power supply
	One power supply load for regulation
System motherboard testing[4]	
PCI-SIG Compliance Base Board (order from www.pcisig.com/specifications/ordering_information)	
ST1847 (www.fairviewmicrowave.com) or equivalent	SMP 50 Ω terminators, one pair for all CLB lanes not probed
N2823A	Phased-matched cable pair, 2.92 mm, 1 m length, 35 GHz
80350960 (Huber+Suhner)	Two SMA-SMP minibend cables
71L-191-321-01000 (Rosenberger) or equivalent	Two SMA (m) to SMP (f) cables for REFCLK probing
N2802A	Two InfiniiMax III/III+ 25 GHz probe amplifiers for tests using only two oscilloscope channels
N5444A	Two InfiniiMax III 2.92 mm/3.5 mm/SMA probe head for tests using only two oscilloscope channels
Semiconductor device testing	
Semiconductor (ASIC) device (BASE spec)	
N2823A	Phased-matched cable pair, 2.92 mm, 1 m length, 35 GHz
N2802A	25 GHz InfiniiMax III probe with 26 GHz solder-in probe head (N2836A)
Optional (for all types of testing)	
11667B	Power splitter, DC to 26.5 GHz, 3.5 mm (f) connectors
11636B	Power divider, DC to 26.5 GHz, 3.5 mm (f) connectors
1250-1159	Three SMA (m - m) adapters
8493B	Coaxial attenuator (3, 6, 10, 20 or 30 dB), DC to 18 GHz, SMA connector

Table 2. Recommended test accessories.

[4] Requires a 4 channel oscilloscope or (if using only two channels) two InfiniiMax II or InfiniiMax III/+ probe amplifiers and SMA/3.5 mm differential probe heads of the appropriate bandwidth for the PCIe data rate you intend to test.

Tests Performed

The PCI Express electrical performance validation and compliance software performs the following tests as per the PCI Express 1.0a and 1.1 electrical specifications for add-in cards and motherboard systems as documented in Section 4 of the base specification (“PHY”) and Section 4 of the card electromechanical specification (“EM”). For reference, the tests performed by the SigTest application are also noted.

For Gen2 testing coverage, the PCI-SIG decided not to create checklist, as was done for Gen1. For test coverage refer to section 4.7.2. Table 4-8 of the PCI Express 2.0 Card Electromechanical Specification.

For PCI Express 3.0, test coverage includes items listed on table 4-18 under section 4.3.3 of the PCI Express 3.0 Base Specification.

Assertion no.	Description	Keysight PCI Express	SigTest
Transmitter tests			
PHY.3.1#26	DC common mode voltage	Y	N
PHY.3.2#1	De-emphasis on multiple bits same polarity in succession	Y	N
PHY.3.2#2	Transition bit voltage	Y	N
PHY.3.3#1	Transmitter eye diagram	Y	N
PHY.3.3#2	Unit interval without SSC variations	Y	N
PHY.3.3#3	Minimum D+/D- output rise/fall time	Y	N
PHY.3.3#4	Jitter median to max deviation	Y	N
PHY.3.3#5	Maximum RMS AC common mode voltage	Y	N
PHY.3.3#9	Minimum eye width	Y	N
Receiver tests			
PHY.3.4#1	Minimum receiver eye diagram	Y [5]	N
PHY.3.4#2	AC peak common mode input voltage	Y [5]	N
PHY.3.4#6	Jitter median to max deviation input	Y [5]	N
System board (connector) tests			
EM.4#4	Minimum jitter	Y [6]	Y
EM.4#20	Transmitter path eye diagram	Y [6]	Y
Reference clock (connector) tests			
PHY.3.3#2	Phase jitter	Y	N/A [5]
PHY.3.3#1	Rising edge rate	Y	N/A
PHY.3.3#1	Falling edge rate	Y	N/A
PHY.3.3#4	Differential input high voltage	Y	N/A
PHY.3.3#4	Differential input low voltage	Y	N/A
PHY.3.3#9	Average clock period	Y	N/A
PHY.3.2#2	Duty cycle	Y	N/A
Add-in card (connector) tests			
EM.4#13	Minimum jitter	Y	Y
EM.4#19	Transmitter path eye diagram	Y	Y

Table 3.

[5] Receiver tests provided by the Keysight PCI Express software are listed under the PCIe 1.x or 2.0 test tabs do not validate the receiver’s tolerance or ability to correctly receive data. They validate the signal at the receiver against specified tolerances.

[6] Requires a 4 channel oscilloscope or (if using only two channels) two Infiniimax or InfiniiMax III/+ probe amplifiers and SMA/3.5 mm differential probe heads of the appropriate bandwidth for the PCIe data rate you intend to test.

Ordering Information

Required hardware and software

- D9040PCIC is compatible with UXR Series and Z-Series, V-Series, Q-Series, X-Series and 9000A series oscilloscopes with Infiniium software version 6.30 or greater.
- D9040PCIC is compatible for 2.5G and reference clock tests only on the S-Series oscilloscope.
- D9040PCIC requires that your oscilloscope be licensed for either the D9110DMBA De-Embedding or D9120ASIA Advanced Signal Integrity software tool.

Flexible software licensing and KeysightCare software support subscriptions

Keysight offers a variety of flexible licensing options to fit your needs and budget. Choose your license term, license type, and KeysightCare software support subscription.

License terms

- **Perpetual** – Perpetual licenses can be used indefinitely.
- **Time-based** – Time-based licenses can be used through the term of the license only (6, 12, 24, or 36 months).

License types

- **Node-locked** – License can be used on one specified instrument/computer.
- **Transportable** – License can be used on one instrument/computer at a time but may be transferred to another using Keysight Software Manager (internet connection required).
- **USB Portable** – License can be used on one instrument/computer at a time but may be transferred to another using a certified USB dongle (available for additional purchase with Keysight part number E8900-D10).
- **Floating (single site)** – Networked instruments/computers can access a license from a server one at a time. Multiple licenses can be purchased for concurrent usage.

KeysightCare software support subscriptions

Perpetual licenses are sold with a 12 (default), 24, 36, or 60-month software support subscription. Support subscriptions can be renewed for a fee after that.

Time-based licenses include a software support subscription through the term of the license.

Selecting your license

- **Step 1.** Choose your software product (eg. D9040PCIC).
- **Step 2.** Choose your license term: perpetual or time-based.
- **Step 3.** Choose your license type: node-locked, transportable, USB portable, or floating.
- **Step 4.** Depending on the license term, choose your support subscription duration.

If you are interested in obtaining a quote for this product, please contact your Keysight representative for pricing and availability.

Subscription based Compliance Test Software Suites

A new ownership model of multiple Compliance Test Software Applications is now available.

With this new subscription based model, the PCI Express software suites bundle the Compliance Test Software Applications under a model number. Using a subscription based ownership, you can enjoy all the test software features covered under PCI Express across multiple generations and variants.

Software support and continuity

Under the subscription plan, software support is made available with no extra support cost. Ensuring your software always stays up to date with the latest enhancements and measurement standards while having access to our team of technical experts when you need support.

On top of that all upgrades are made available to you as the PCI Express standards progresses with no additional costs.

Subscription based Compliance Test Software Suites

Each suite comes with a 12, 24, or 36-month software suite subscription.

Model number	Options available
SW00PCIE PCI Express Validation License	PCI Express Gen 4 TX Test (D9040PCIC) PCI Express Gen 5 TX Test (D9050PCIC)
SW02PCIE PCI Express Full TX Test Suite	PCI Express Gen 4 TX Test (D9040PCIC) PCI Express Gen 5 TX Test (D9050PCIC) Advanced PCI Express Protocol Decode (D9010PCIP)